

## CMOS 8-bit Single Chip Microcomputer

### Description

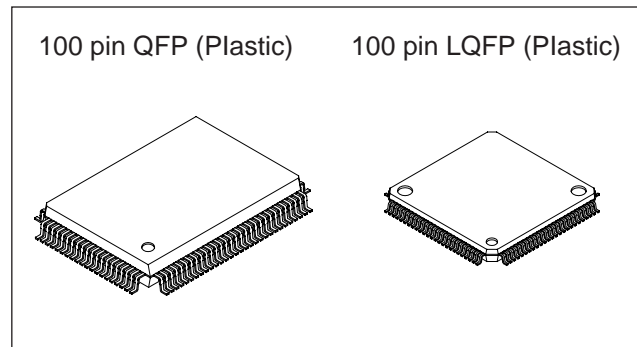
The CXP873P60 is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, VISS/VASS circuit, 32kHz timer/event counter, remote control receiving circuit, general purpose prescaler, HSYNC counter, VCR vertical sync separation circuit and the measurement circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also the CXP873P60 provides sleep/stop function which enables to lower power consumption and ultra-low speed instruction mode in 32kHz operation.

Incorporating a one-time PROM, the CXP873P60 has an equivalent function to the CXP87360, and is suitable for evaluation in system development and for the production of small amounts.

### Features

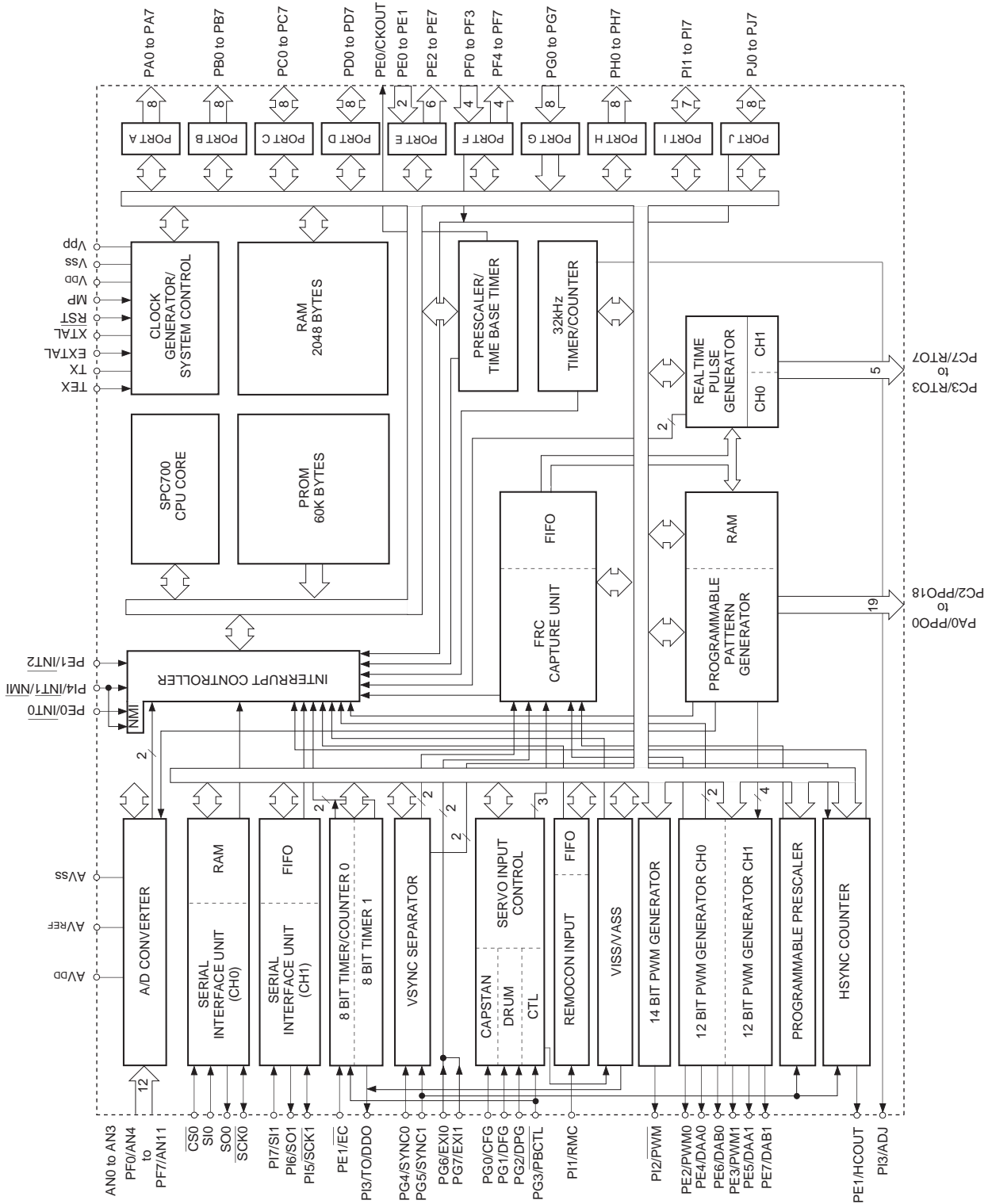
- A wide instruction set (213 instructions) which cover various types of data
  - 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
  - 250ns at 16MHz operation (4.5V to 5.5V)
  - 333ns at 12MHz operation (3.0V to 5.5V)
  - 122µs at 32kHz operation
- Incorporated PROM capacity 60K bytes
- Incorporated RAM capacity 2048 bytes
- Peripheral functions
  - A/D converter 8-bit, 12-channel, successive approximation system (Conversion time 20.0µs/16MHz)
  - Serial interface Incorporated buffer RAM (1 to 32 bytes auto transfer) 1-channel  
Incorporated 8-bit and 8-stage FIFO for data (1 to 8 bytes auto transfer) 1-channel
  - Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
  - High precision timing pattern generator PPG 19-pin 32-stage programmable  
RTG 5-pin 2-channel
  - PWM/DA gate output PWM 12-bit, 2-channel (Repetitive frequency 62kHz/16MHz)  
DA gate pulse output 13-bit, 4-channel  
Capstan FG, Drum FG/PG, CTL input
  - Servo input control Incorporated 26-bit and 8-stage FIFO
  - VSYNC separator 14-bit, 1-channel
  - FRC capture unit Pulse duty auto detection circuit
  - PWM output 8-bit pulse measurement counter with on-chip, 6-stage FIFO
  - VISS/VASS circuit 7-bit (SYNC1 input frequency divided, FRC capture possible)
  - Remote control receiving circuit 12-bit event counter (Counts SYNC1 input.)
  - General purpose prescaler 21 factors, 15 vectors, multi-interruption possible
  - HSYNC counter SLEEP/STOP
- Interruption 100-pin plastic QFP/LQFP
- Standby mode
- Package



### Structure

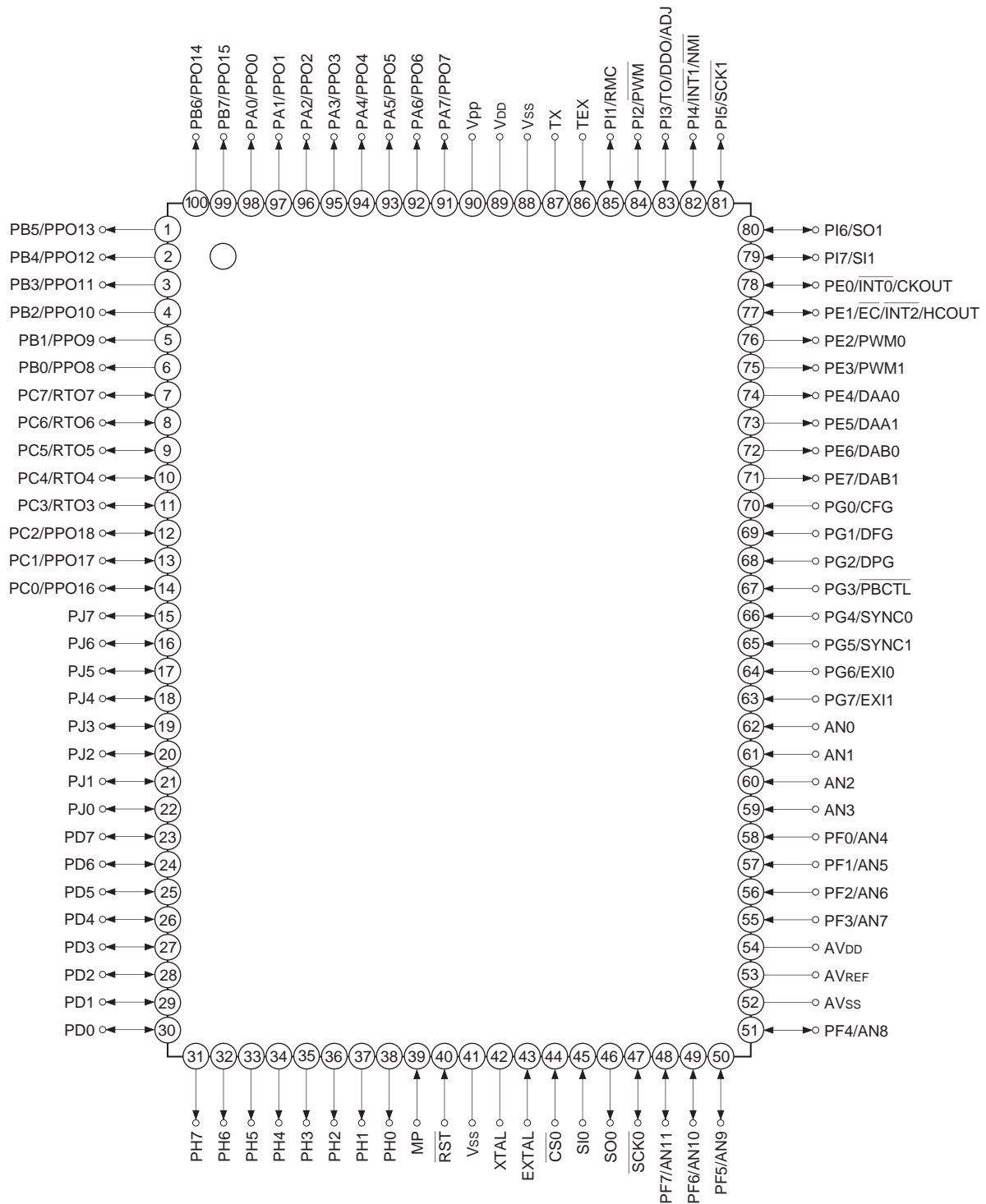
Silicon gate CMOS IC

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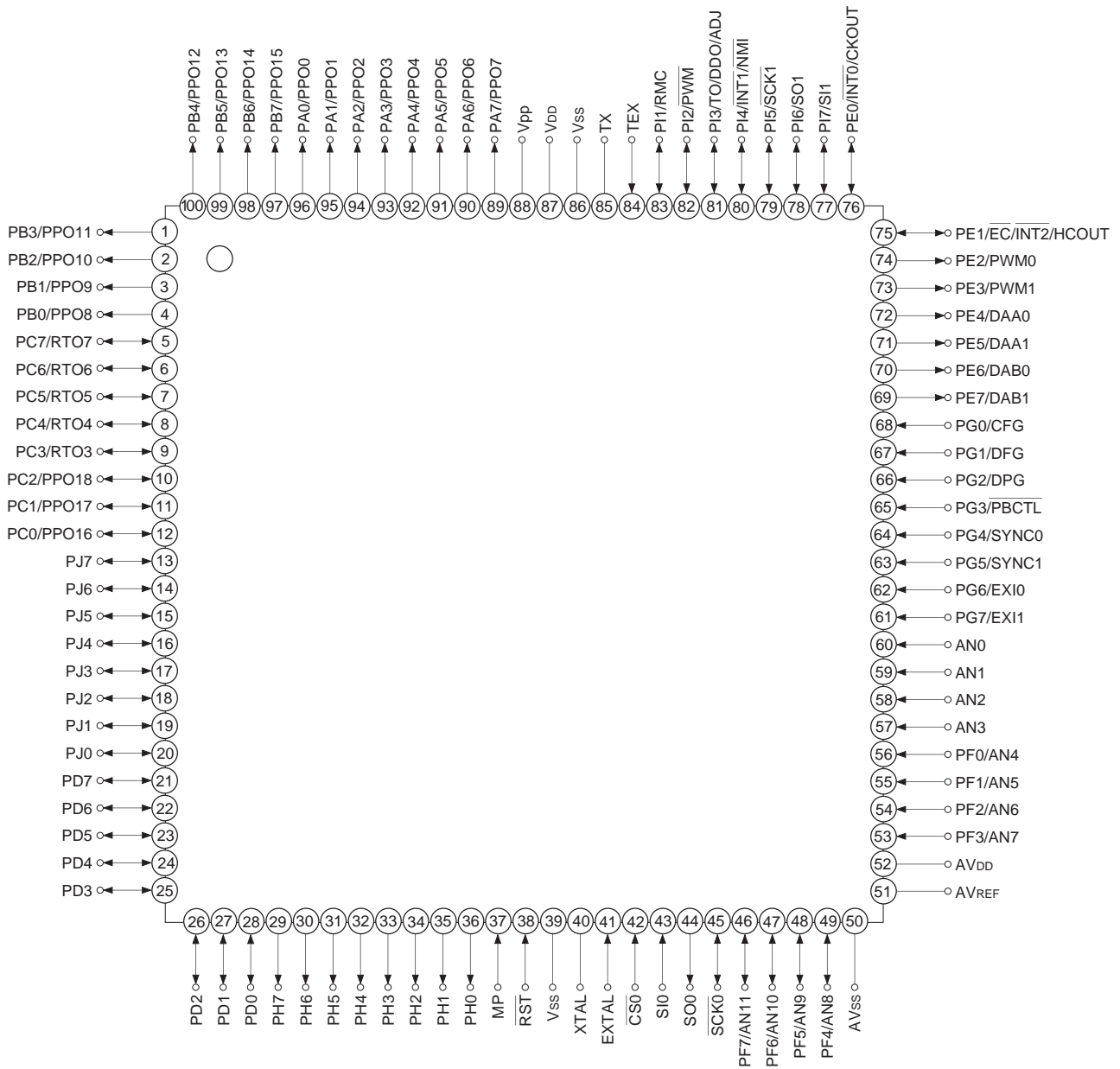
Block Diagram

Pin Configuration 1 (Top View) 100-pin QFP package



- Note)** 1. Vpp (Pin 90) is always connected to V<sub>DD</sub>.  
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100-pin LQFP package



- Note** 1. Vpp (Pin 88) is always connected to Vdd.  
 2. Vss (Pins 39 and 86) are both connected to GND.

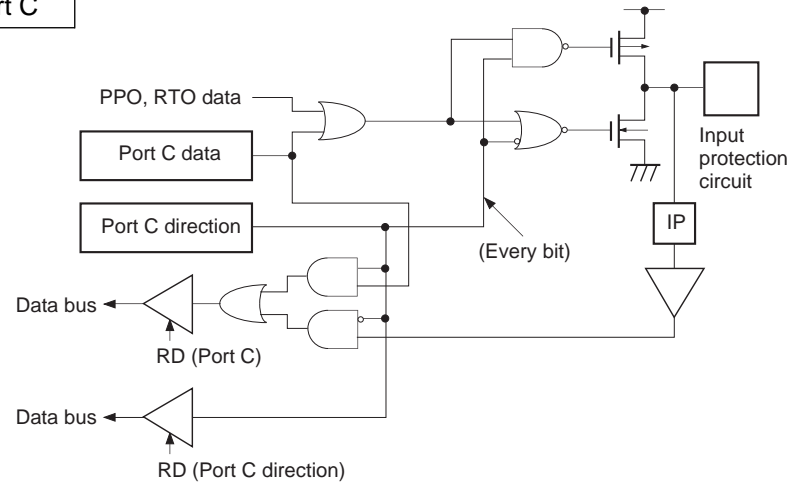
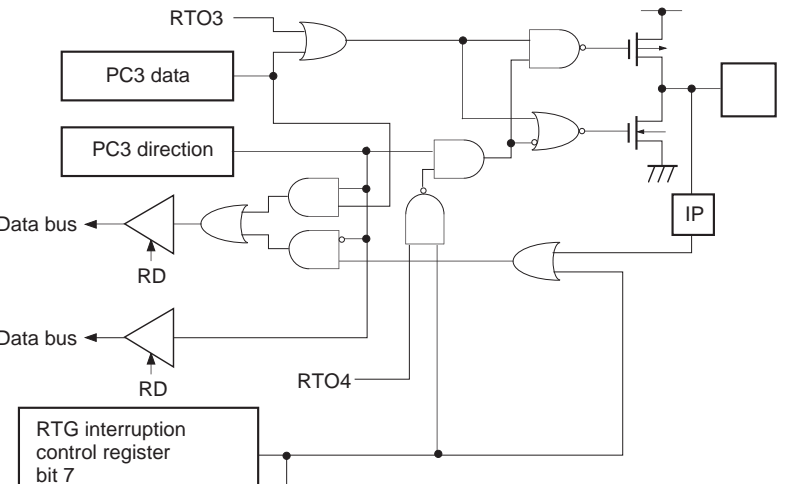
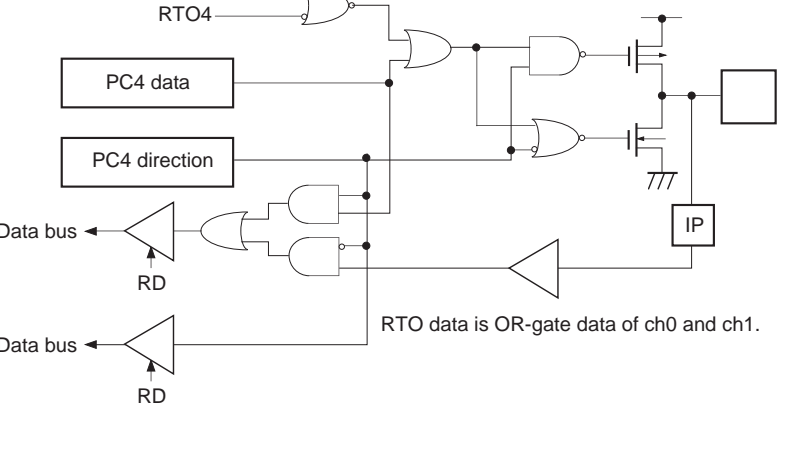
Pin Description

Symbol	I/O	Description			
PA0/PPO0 to PA7/PPO7	Output/Real time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins) PB0 and PB2 can be 3-state controlled with PPG.		
PB0/PPO8 to PB7/PPO15	Output/Real time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)			
PC0/PPO16 to PC2/PPO18	I/O/Real time output	(Port C) 8-bit I/O port, enables to specify I/O by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)			
PC3/RTO3 to PC7/RTO7	I/O/Real time output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)		
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify I/O by 4-bit unit. Enables to drive 12mA sink current. (8 pins)			
PE0/ $\overline{\text{INT0}}$ /CKOUT	Input/Input/Output	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.		
			PC3 can be 3-state controlled with RTG. System clock frequency division output.		
PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$ /HCOUT	Input/Input/Input/Output		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.	Coincidence signal output of HSYNC counter.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)		
PE3/PWM1	Output/Output				
PE4/DAA0	Output/Output				
PE5/DAA1	Output/Output				
PE6/DAB0	Output/Output		DA gate pulse output pins. (4 pins)		
PE7/DAB1	Output/Output				
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)			
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)			
PF4/AN8 to PF7/AN11	Output/Input				
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.			
SO0	Output	Serial data (CH0) output pin.			
SI0	Input	Serial data (CH0) input pin.			
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.			

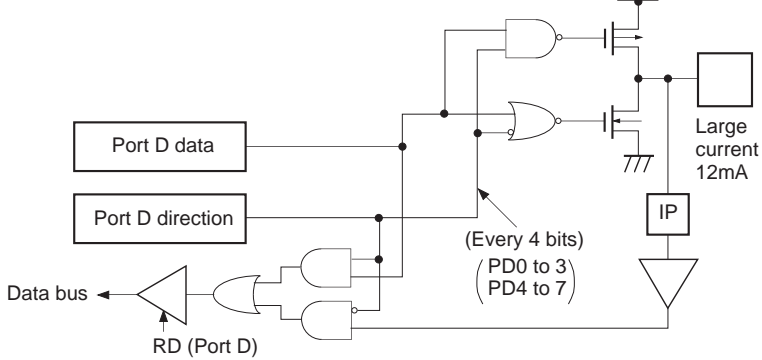
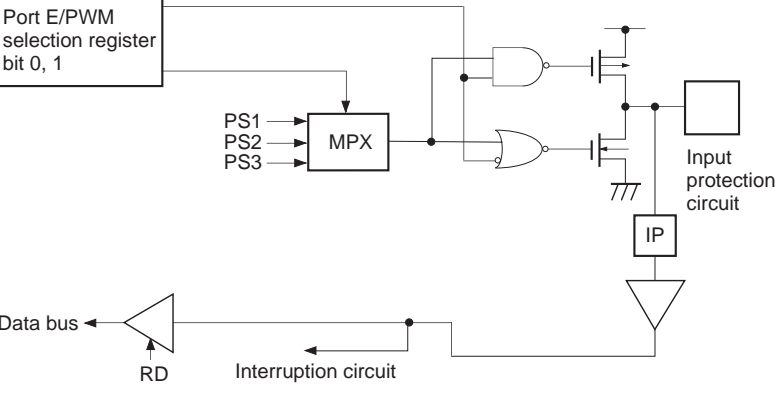
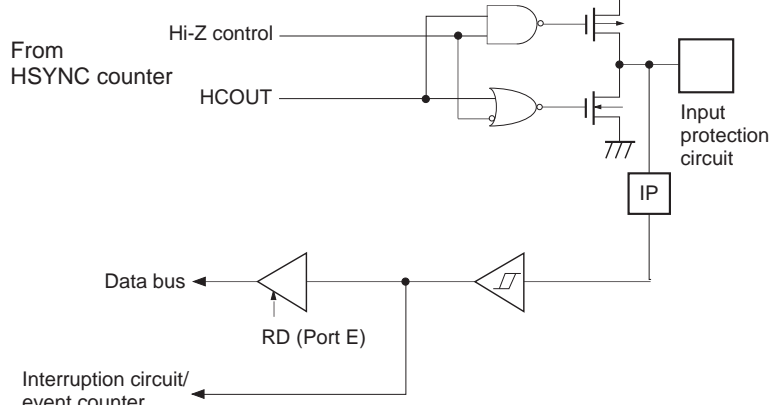
Symbol	I/O	Description	
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input/Input		Drum FG input pin.
PG2/DPG	Input/Input		Drum PG input pin.
PG3/ $\overline{\text{PBCTL}}$	Input/Input		Playback CTL pulse input pin. External event input pin of timer/counter.
PG4/SYNC0	Input/Input		Composite sync signal input pin.
PG5/SYNC1	Input/Input		
PG6/EXI0	Input/Input		External input pin to FRC capture unit.
PG7/EXI1	Input/Input		
PH0 to PH7	Output	(Port H) 8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output. (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be specified by bit unit. (7 pins)	Remote control receiving circuit input pin.
PI2/ $\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.
PI3/TO/ DDO/ADJ	I/O/Output/ Output/Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.
PI4/ $\overline{\text{INT1}}$ / NMI	I/O/Input/Input		Input pin to request external interruption and non-maskable interruption. Active when falling edge.
PI5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/Output		Serial data (CH1) output pin.
PI7/SI1	I/O/Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
$\overline{\text{RST}}$	Input	System reset pin of active "L" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV <sub>DD</sub>		Positive power supply pin of A/D converter.	
AV <sub>REF</sub>	Input	Reference voltage input pin of A/D converter.	
AV <sub>SS</sub>		GND pin of A/D converter.	
V <sub>DD</sub>		Positive power supply pin.	
V <sub>pp</sub>		Positive power supply pin for incorporated PROM writing. In normal operation, connect to V <sub>DD</sub> .	
V <sub>SS</sub>		GND pin. Connect both V <sub>SS</sub> pins to GND.	

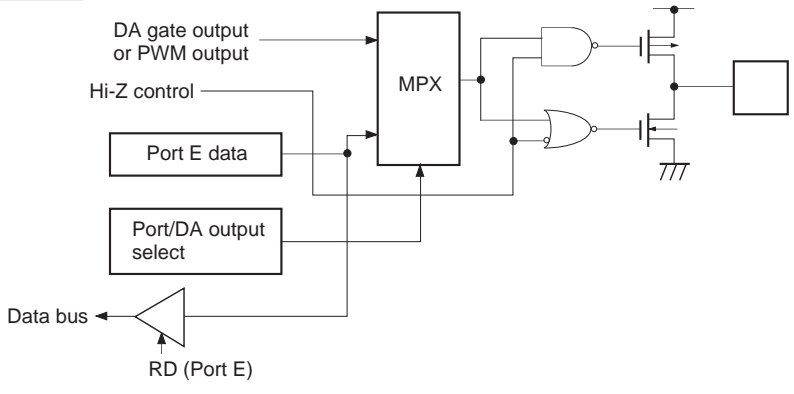
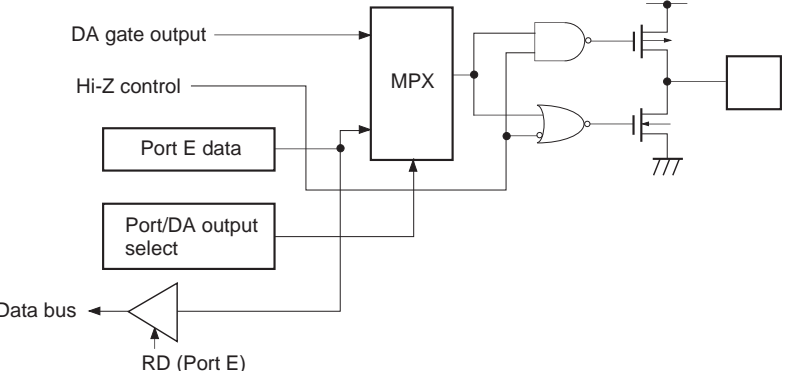
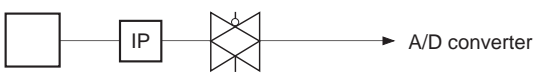
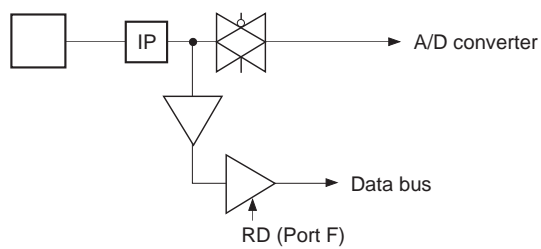
Input/Output Circuit Formats for Pins

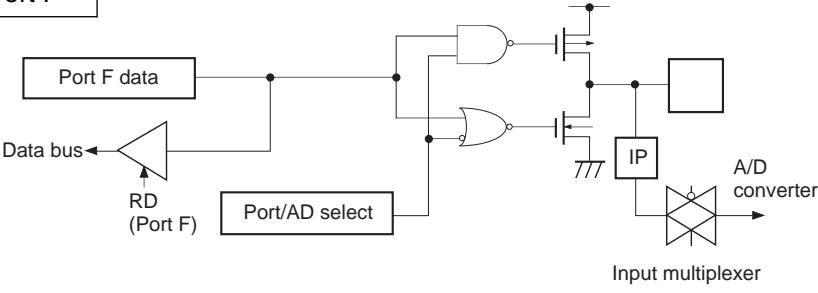
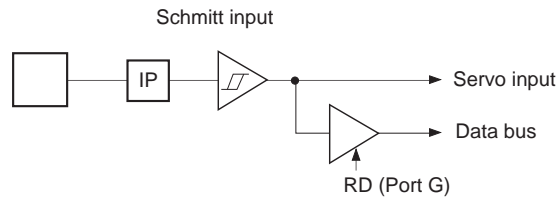
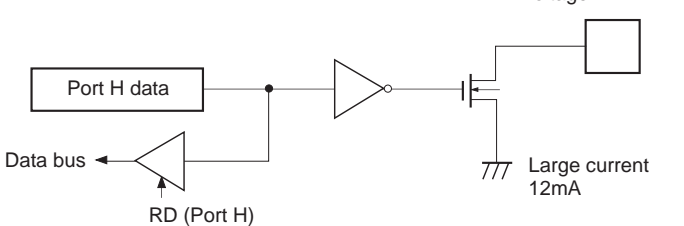
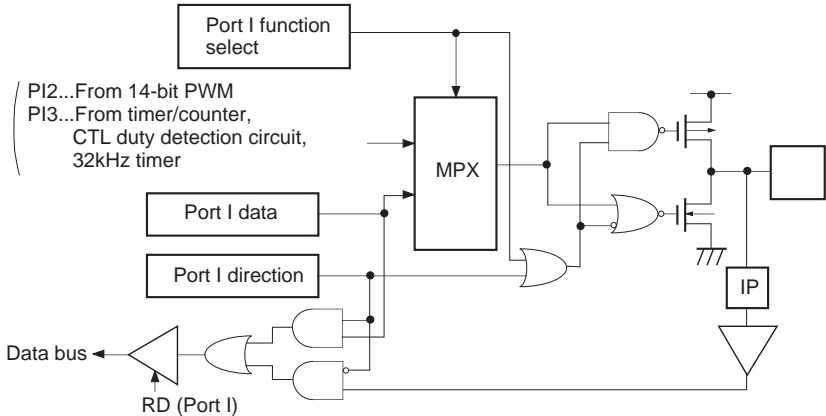
Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0 /PPO0 to PA7/PPO7</p> <p>PB4/PPO12 to PB7/PPO15</p> <p>12 pins</p>	<p>PPO data</p> <p>Port A or Port B</p> <p>Data bus</p> <p>RD</p> <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>PB0 /PPO8 PB2/PPO10</p> <p>2 pins</p>	<p>PPO8 or PPO10</p> <p>PB0 or PB2 data</p> <p>RD</p> <p>Data bus</p> <p>Output becomes active from high impedance by data writing to port register.</p> <p>PPO9 or PPO11</p>	<p>Hi-Z</p>
<p>PB1/PPO9 PB3/PPO11</p> <p>2 pins</p>	<p>PPG control status register bit 0 3-state control selection</p> <p>PPO9 or PPO11</p> <p>PB1 or PB3 data</p> <p>Data bus</p> <p>RD</p> <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PC0/PPO16 to PC2/PPO18</p> <p>PC5/RTO5 to PC7/RTO7</p> <p>6 pins</p>	<p>Port C</p> 	<p>Hi-Z</p>
<p>PC3/RTO3</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>PC4/RTO4</p> <p>1 pin</p>	 <p>RTO data is OR-gate data of ch0 and ch1.</p>	<p>Hi-Z</p>

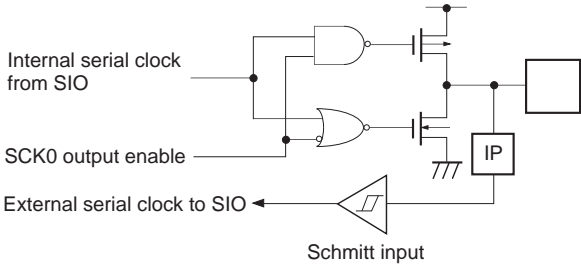
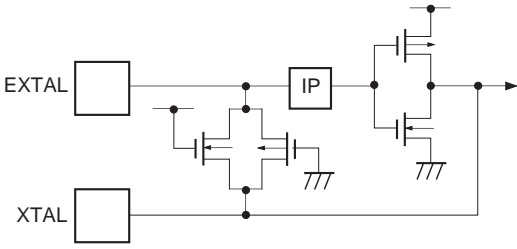
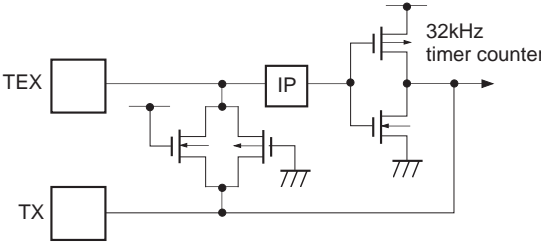
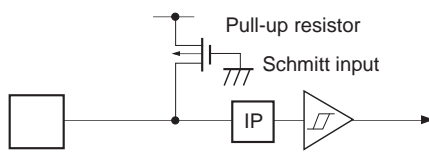
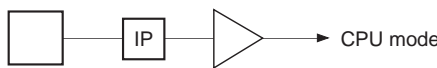


Pin	Circuit format	When reset
<p>PD0 to PD7</p> <p>8 pins</p>	<p>Port D</p>  <p>Port D data</p> <p>Port D direction</p> <p>Data bus</p> <p>RD (Port D)</p> <p>(Every 4 bits) (PD0 to 3) (PD4 to 7)</p> <p>Large current 12mA</p> <p>IP</p>	<p>Hi-Z</p>
<p>PE0/<math>\overline{\text{INT0}}</math>/ CKOUT</p> <p>1 pin</p>	<p>Port E</p>  <p>Port E/PWM selection register bit 0, 1</p> <p>PS1</p> <p>PS2</p> <p>PS3</p> <p>MPX</p> <p>Data bus</p> <p>RD</p> <p>Input protection circuit</p> <p>IP</p> <p>Interruption circuit</p>	<p>Hi-Z</p>
<p>PE1/<math>\overline{\text{EC}}</math>/<math>\overline{\text{INT2}}</math></p> <p>1 pin</p>	<p>Port E</p>  <p>From HSYNC counter</p> <p>Hi-Z control</p> <p>HCOUNT</p> <p>Data bus</p> <p>RD (Port E)</p> <p>Input protection circuit</p> <p>IP</p> <p>Interruption circuit/ event counter</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p> 	<p>H level</p>
<p>AN0 to AN3</p> <p>4 pins</p>	<p>Input multiplexer</p> 	<p>Hi-Z</p>
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p> <p>Input multiplexer</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p>  <p>Port F data</p> <p>Data bus</p> <p>RD (Port F)</p> <p>Port/AD select</p> <p>Input multiplexer</p> <p>A/D converter</p>	<p>Hi-Z</p>
<p>PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1</p> <p>8 pins</p>	<p>Port G</p>  <p>Schmitt input</p> <p>IP</p> <p>Servo input</p> <p>Data bus</p> <p>RD (Port G)</p> <p>Note) For PG4 and PG5 input format, there are CMOS schmitt input and TTL schmitt input with product.</p>	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>Port H data</p> <p>Data bus</p> <p>RD (Port H)</p> <p>Medium withstand voltage 12V</p> <p>Large current 12mA</p>	<p>Hi-Z</p>
<p>PI2/PWM PI3/TO/ DDO/ADJ</p> <p>2 pins</p>	<p>Port I</p>  <p>Port I function select</p> <p>MPX</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p> <p>(PI2...From 14-bit PWM PI3...From timer/counter, CTL duty detection circuit, 32kHz timer</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
PI1/RMC PI4/INT1/NMI PI7/SI1  3 pins	<p>Port I</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Schmitt input</p> <p>IP</p> <p>PI1...To remote control circuit                      PI4...To interruption circuit                      PI7...To serial CH1</p>	Hi-Z
PI5/SCK1 PI6/SO1  2 pins	<p>Port I</p> <p>Port I function select</p> <p>From serial CH1</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Note)                      (PI5 is schmitt input                      PI6 is inverter input)</p> <p>To serial CH1</p> <p>IP</p>	Hi-Z
PJ0 to PJ7  8 pins	<p>Port J</p> <p>Port J data</p> <p>Port J direction</p> <p>Data bus</p> <p>RD (Port J)</p> <p>Edge detection</p> <p>Standby release</p> <p>Data bus</p> <p>RD</p> <p>IP</p>	Hi-Z
$\overline{\text{CS0}}$ SI0  2 pins	<p>Schmitt input</p> <p>To SIO</p> <p>IP</p>	Hi-Z
SO0  1 pin	<p>SO0 from SIO</p> <p>SO0 output enable</p> <p>IP</p>	Hi-Z

Pin	Circuit format	When reset
<p><math>\overline{\text{SCK0}}</math></p> <p>1 pin</p>	 <p>Internal serial clock from SIO</p> <p>SCK0 output enable</p> <p>External serial clock to SIO</p> <p>Schmitt input</p> <p>IP</p>	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop.</li> </ul>	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level.</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Schmitt input</p> <p>IP</p>	<p>L level</p>
<p>MP</p> <p>1 pin</p>	 <p>IP</p> <p>Schmitt input</p> <p>CPU mode</p>	<p>Hi-Z</p>

## Absolute Maximum Ratings

(V<sub>SS</sub>=0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	V <sub>pp</sub>	-0.3 to +13	V	PROM version only
	AV <sub>DD</sub>	AV <sub>SS</sub> to +7.0* <sup>1</sup>	V	
	AV <sub>SS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>2</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>2</sup>	V	
Medium withstand output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	PH pin
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of output pins
Low level output current	I <sub>OL</sub>	15	mA	Other than large current output pins: per pin
	I <sub>OLC</sub>	20	mA	Large current port pin* <sup>3</sup> : per pin
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of output pins
Operating temperature	T <sub>opr</sub>	-10 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	QFP package type
		380		LQFP package type

\*1) AV<sub>DD</sub> and V<sub>DD</sub> should be set to a same voltage.

\*2) V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub>+0.3V.

\*3) The large current operation transistors are the N-CH transistors of the PD and PH ports.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub>=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	3.0	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.0	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV <sub>DD</sub>	3.0	5.5	V	*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
			5.5	V	CMOS schmitt input*7
	V <sub>IHTS</sub>	2.2	5.5	V	TTL schmitt input*4
	V <sub>IHEX</sub>	V <sub>DD</sub> -0.4	V <sub>DD</sub> +0.3	V	EXTAL pin*5, *8 and TEX pin*6, *8
			V <sub>DD</sub> -0.2	V <sub>DD</sub> +0.2	V
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*2, *8
		0	0.2V <sub>DD</sub>	V	*2, *9
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
	V <sub>ILTS</sub>	0	0.8	V	TTL schmitt input*4
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*5, *8 and TEX pin*6, *8
			0.2	V	EXTAL pin*5, *9 and TEX pin*6, *9
Operating temperature	T <sub>opr</sub>	-10	+75	°C	

\*1) AV<sub>DD</sub> and V<sub>DD</sub> should be set to a same voltage.

\*2) Normal input port (each pin of PC, PD, PF0 to PF3, PG, PI and PJ), MP pin.

\*3) Each pin of  $\overline{\text{SCK0}}$ ,  $\overline{\text{RST}}$ , PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$ , PI1/RMC, PI4/ $\overline{\text{INT1}}$ /NMI, PI5/ $\overline{\text{SCK1}}$  and PI7/SI1.

\*4) Each pin of PG4 and PG5 (When TTL schmitt input is selected for the product)

\*5) It specifies only when the external clock is input.

\*6) It specifies only when the external event count clock is input.

\*7) Each pin of  $\overline{\text{CS0}}$ , SI0, and PG (For PG4 and PG5, when CMOS schmitt input is selected for the product.)

\*8) In case of 4.5 to 5.5V supply voltage (V<sub>DD</sub>).

\*9) In case of 3.0 to 3.6V supply voltage (V<sub>DD</sub>).

**Electrical Characteristics**

**DC Characteristics** ( $V_{DD} = 4.5$  to  $5.5V$ )

( $T_a = -10$  to  $+75^\circ C$ ,  $V_{SS} = 0V$ )

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	$V_{OH}$	PA to PD, PE2 to PE7, PF4 to PF7, PH ( $V_{OL}$ only)	$V_{DD} = 4.5V$ , $I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V$ , $I_{OH} = -1.2mA$	3.5			V
Low level output voltage	$V_{OL}$	PI1 to PI7, PJ, SO0, SCK0	$V_{DD} = 4.5V$ , $I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V$ , $I_{OL} = 3.6mA$			0.6	V
		PD, PH	$V_{DD} = 4.5V$ , $I_{OL} = 12.0mA$			1.5	V
Input current	$I_{IHE}$	EXTAL	$V_{DD} = 5.5V$ , $V_{IH} = 5.5V$	0.5		40	$\mu A$
	$I_{ILE}$		$V_{DD} = 5.5V$ , $V_{IL} = 0.4V$	-0.5		-40	$\mu A$
	$I_{IHT}$	TEX	$V_{DD} = 5.5V$ , $V_{IH} = 5.5V$	0.1		10	$\mu A$
	$I_{ILT}$		$V_{DD} = 5.5V$ , $V_{IL} = 0.4V$	-0.1		-10	$\mu A$
	$I_{ILR}$		$\overline{RST}$	$V_{DD} = 5.5V$ , $V_{IL} = 0.4V$	-1.5		-400
I/O leakage current	$I_{IZ}$	PA to PG, PI, PJ, MP, AN0 to AN3, CS0, SI0, SO0, SCK0	$V_{DD} = 5.5V$ , $V_I = 0, 5.5V$			$\pm 10$	$\mu A$
Open drain output leakage current (N-CH Tr OFF in state)	$I_{LOH}$	PH	$V_{DD} = 5.5V$ , $V_{OH} = 12V$			50	$\mu A$
Supply current*1	$I_{DD1}$	$V_{DD}$	16MHz crystal oscillation ( $C_1 = C_2 = 15pF$ )		28	50	mA
			$V_{DD} = 5V \pm 0.5V^{*2}$				
	$I_{DDS1}$		SLEEP mode		1.7	8	mA
			$V_{DD} = 5V \pm 0.5V$				
	$I_{DD2}$		32kHz crystal oscillation ( $C_1 = C_2 = 47pF$ )		0.7	2	mA
			$V_{DD} = 3V \pm 0.3V$				
	$I_{DDS2}$		SLEEP mode		8	35	$\mu A$
$V_{DD} = 3V \pm 0.3V$							
$I_{DDS3}$	STOP mode (EXTAL and TEX pins oscillation stop)				30	$\mu A$	
$V_{DD} = 5V \pm 0.5V$							
Input capacity	$C_{IN}$	Other than $V_{DD}$ , $V_{SS}$ , $AV_{DD}$ , and $AV_{SS}$	Clock 1MHz 0V other than the measured pins		10	20	pF

\*1) When entire output pins are open.

\*2) When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).



DC Characteristics (V<sub>DD</sub>=3.0 to 3.6V)

(T<sub>a</sub>=-10 to +75°C, V<sub>SS</sub>=0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V <sub>OH</sub>	PA to PD, PE2 to PE7, PF4 to PF7,	V <sub>DD</sub> =3.0V, I <sub>OH</sub> =-0.15mA	2.7			V
			V <sub>DD</sub> =3.0V, I <sub>OH</sub> =0.5mA	2.3			V
Low level output voltage	V <sub>OL</sub>	PH (V <sub>OL</sub> only) PI1 to PI7	V <sub>DD</sub> =3.0V, I <sub>OL</sub> =1.2mA			0.3	V
			V <sub>DD</sub> =3.0V, I <sub>OL</sub> =1.6mA			0.5	V
		PJ, SO0, SCK0	V <sub>DD</sub> =3.0V, I <sub>OL</sub> =5mA			1.0	V
Input current	I <sub>IHE</sub>	EXTAL	V <sub>DD</sub> =3.6V, V <sub>IH</sub> =3.6V	0.3		20	μA
	I <sub>ILE</sub>		V <sub>DD</sub> =3.6V, V <sub>IL</sub> =0.3V	-0.3		-20	μA
	I <sub>IHT</sub>	TEX	V <sub>DD</sub> =3.6V, V <sub>IH</sub> =3.6V	0.1		10	μA
	I <sub>ILT</sub>		V <sub>DD</sub> =3.6V, V <sub>IL</sub> =0.3V	-0.1		-10	μA
	I <sub>ILR</sub>	RST	V <sub>DD</sub> =3.6V, V <sub>IL</sub> =0.3V	-0.9		-200	μA
I/O leakage current	I <sub>Iz</sub>	PA to PG, PI, PJ, MP AN0 to AN3, CS0, SI0, SO0 SCK0	V <sub>DD</sub> =3.6V, V <sub>I</sub> =0, 3.6V			±10	μA
Open drain output leakage current	I <sub>LOH</sub>	PH	V <sub>DD</sub> =3.6V, V <sub>OH</sub> =12V			50	μA
Supply current*1	I <sub>DD1</sub>	V <sub>DD</sub>	12MHz crystal oscillation (C <sub>1</sub> =C <sub>2</sub> =15pF)		12	30	mA
	I <sub>DDS1</sub>		V <sub>DD</sub> =3.3V±0.3V*2				
			SLEEP mode		0.8	2.5	mA
I <sub>DDS3</sub>	STOP mode (EXTAL and TEX pins oscillation stop)				30	μA	
Input capacity	C <sub>IN</sub>	Other than V <sub>DD</sub> , V <sub>SS</sub> , AV <sub>DD</sub> , and AV <sub>SS</sub>	Clock 1MHz		10	20	pF
			0V other than the measured pins				

\*1) When entire output pins are open.

\*2) When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE<sub>H</sub>) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta=-10 to +75°C, VDD=3.0 to 5.5V, VSS=0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit	
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	VDD = 4.5 to 5.5V	1	16	MHz
					1	12	
System clock input pulse width	tXL, tXH	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	VDD = 4.5 to 5.5V	28		ns
					37.5		
System clock input rise and fall times	tCR, tCF	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns	
Event count clock input pulse width	tEH, tEL	$\overline{EC}$	Fig. 3	tsys x 4*		ns	
Event count clock input rise and fall times	tER, tEF	$\overline{EC}$	Fig. 3		20	ns	
System clock frequency	fc	TEX TX	Fig. 2 VDD=2.7 to 5.5V (32kHz clock applied condition)	32.768		kHz	
Event count clock input pulse width	tTL, tTH	TEX	Fig. 3	10		μs	
Event count clock input rise and fall times	tTR, tTF	TEX	Fig. 3		20	ms	

\* tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Fig. 1. Clock timing

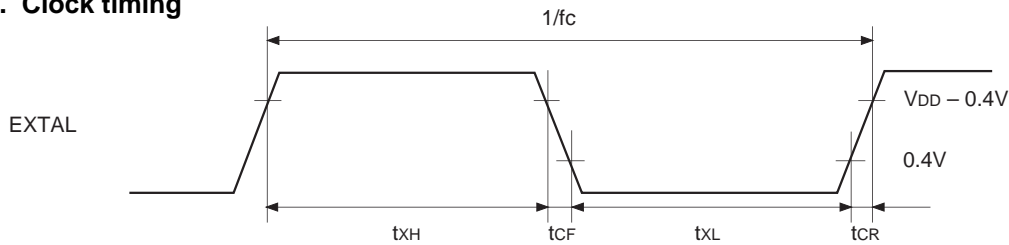


Fig. 2. Clock applied condition

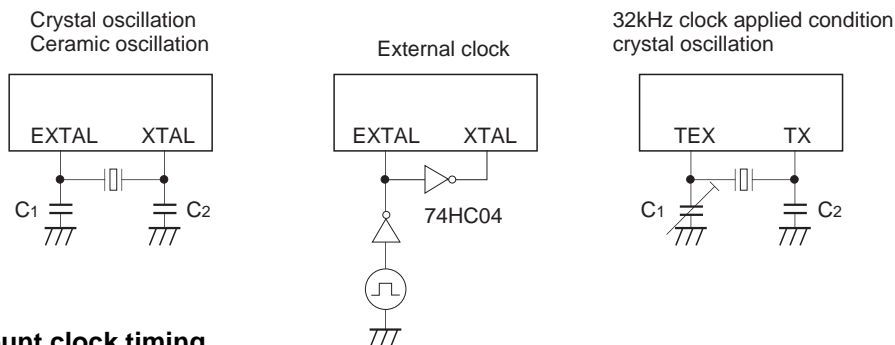
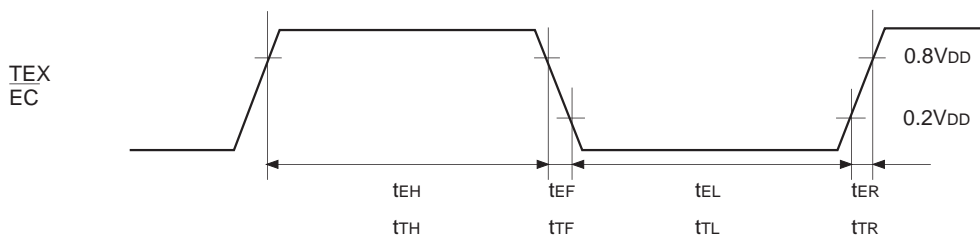


Fig. 3. Event count clock timing



## (2) Serial transfer (CH0)

(Ta=-10 to +75°C, VDD=4.5 to 5.5V, VSS=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	$t_{DCSK}$	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK}$ =output mode)		$t_{sys}+200$	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	$t_{DCSKF}$	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK}$ =output mode)		$t_{sys}+200$	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	$t_{DCSO}$	SO0	Chip select transfer mode		$t_{sys}+200$	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	$t_{DCSOF}$	SO0	Chip select transfer mode		$t_{sys}+200$	ns
$\overline{CS}$ high level width	$t_{WHCS}$	$\overline{CS0}$	Chip select transfer mode	$t_{sys}+200$		ns
$\overline{SCK}$ cycle time	$t_{KCY}$	$\overline{SCK0}$	Input mode	$2t_{sys}+200$		ns
			Output mode	$8000/fc$		ns
$\overline{SCK}$ high and low level widths	$t_{KH}$ $t_{KL}$	$\overline{SCK0}$	Input mode	$t_{sys}+100$		ns
			Output mode	$8000/fc-100$		ns
SI input setup time (against $\overline{SCK} \uparrow$ )	$t_{SIK}$	SI0	$\overline{SCK}$ input mode	$-t_{sys}+100$		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$ )	$t_{KSI}$	SI0	$\overline{SCK}$ input mode	$2t_{sys}+100$		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	$t_{KSO}$	SO0	$\overline{SCK}$ input mode		$2t_{sys}+200$	ns
			$\overline{SCK}$ output mode		100	ns

**Note 1)**  $t_{sys}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{sys}$  [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

**Note 2)**  $\overline{CS}$ ,  $\overline{SCK}$ , SI and SO means each pin of  $\overline{CS} \rightarrow \overline{CS0}$ ,  $\overline{SCK} \rightarrow \overline{SCK0}$ , SI  $\rightarrow$  SI0, and SO  $\rightarrow$  SO0 respectively.

**Note 3)** The load of  $\overline{SCK}$  output mode and SO output delay time is 50pF+1TTL.

## Serial transfer (CH0)

(Ta=-10 to +75°C, VDD=3.0 to 3.6V, VSS=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	$t_{DCSK}$	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK}$ =output mode)		$t_{sys}+250$	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	$t_{DCSKF}$	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK}$ =output mode)		$t_{sys}+200$	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	$t_{DCSO}$	SO0	Chip select transfer mode		$t_{sys}+250$	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	$t_{DCSOF}$	SO0	Chip select transfer mode		$t_{sys}+200$	ns
$\overline{CS}$ high level width	$t_{WHCS}$	$\overline{CS0}$	Chip select transfer mode	$t_{sys}+200$		ns
$\overline{SCK}$ cycle time	$t_{KCY}$	$\overline{SCK0}$	Input mode	$2t_{sys}+200$		ns
			Output mode	$8000/fc$		ns
$\overline{SCK}$ high and low level widths	$t_{KH}$ $t_{KL}$	$\overline{SCK0}$	Input mode	$t_{sys}+100$		ns
			Output mode	$8000/fc-150$		ns
SI input setup time (against $\overline{SCK} \uparrow$ )	$t_{SIK}$	SI0	$\overline{SCK}$ input mode	$-t_{sys}+100$		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$ )	$t_{KSI}$	SI0	$\overline{SCK}$ input mode	$2t_{sys}+100$		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	$t_{KSO}$	SO0	$\overline{SCK}$ input mode		$2t_{sys}+250$	ns
			$\overline{SCK}$ output mode		125	ns

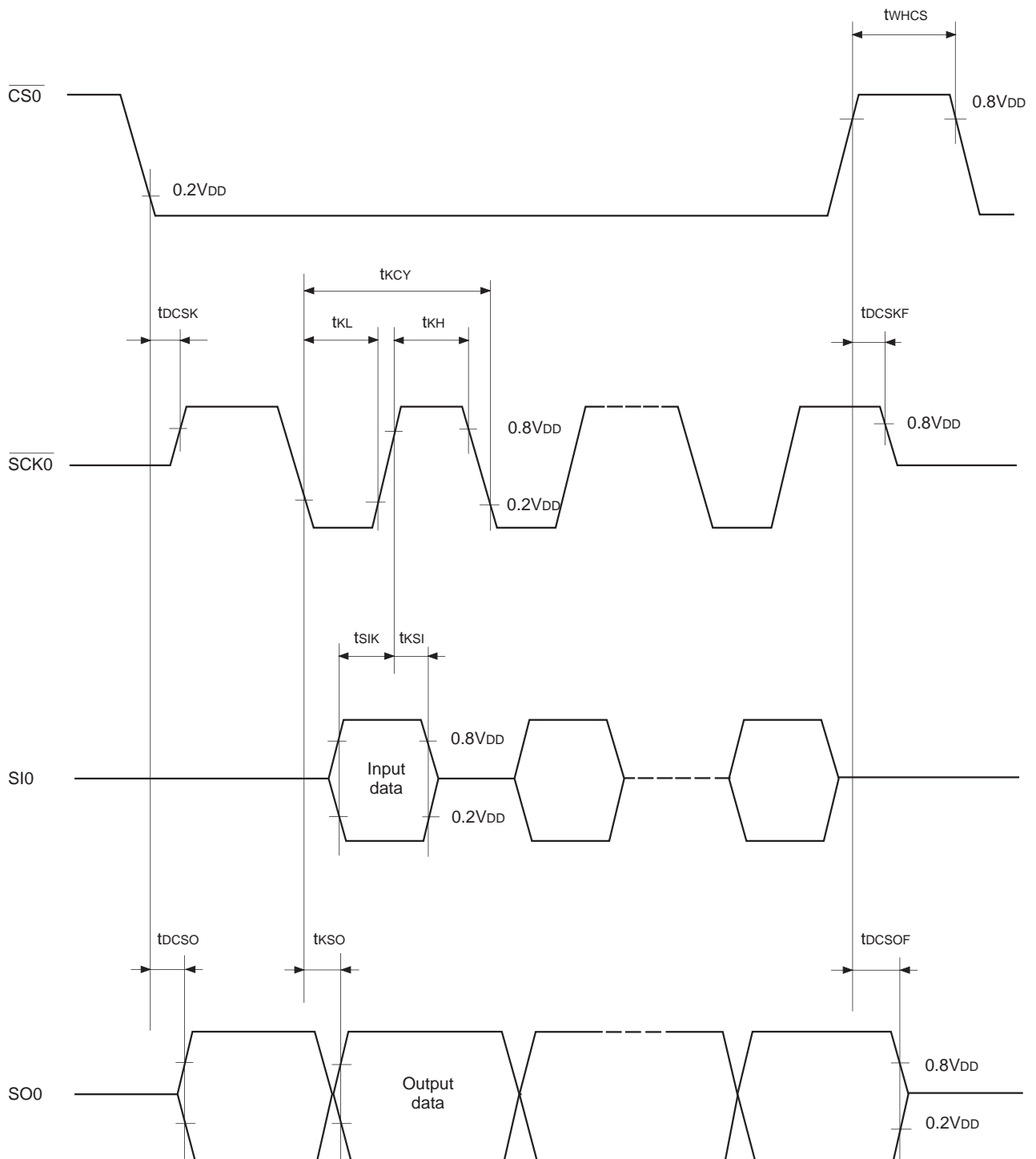
**Note 1)**  $t_{sys}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{sys}$  [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

**Note 2)**  $\overline{CS}$ ,  $\overline{SCK}$ , SI and SO means each pin of  $\overline{CS} \rightarrow \overline{CS0}$ ,  $\overline{SCK} \rightarrow \overline{SCK0}$ , SI  $\rightarrow$  SI0, and SO  $\rightarrow$  SO0 respectively.

**Note 3)** The load of  $\overline{SCK}$  output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



## Serial transfer (CH1) (SIO mode)

(Ta=-10 to +75°C, VDD=4.5 to 5.5V, VSS=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}}+200$		ns
			Output mode	$16000/f_c$		ns
SCK1 high and low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}}+100$		ns
			Output mode	$8000/f_c-100$		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	$t_{\text{SIK}}$	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	$t_{\text{KSI}}$	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}}+200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	$t_{\text{KSO}}$	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}}+200$	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{\text{sys}}$  [ns]=2000/ $f_c$  (Upper 2 bits="00"), 4000/ $f_c$  (Upper 2 bits="01"), 16000/ $f_c$  (Upper 2 bits="11")

**Note 2)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is 50pF+1TTL.

## Serial transfer (CH1) (SIO mode)

(Ta=-10 to +75°C, VDD=3.0 to 3.6V, VSS=0V)

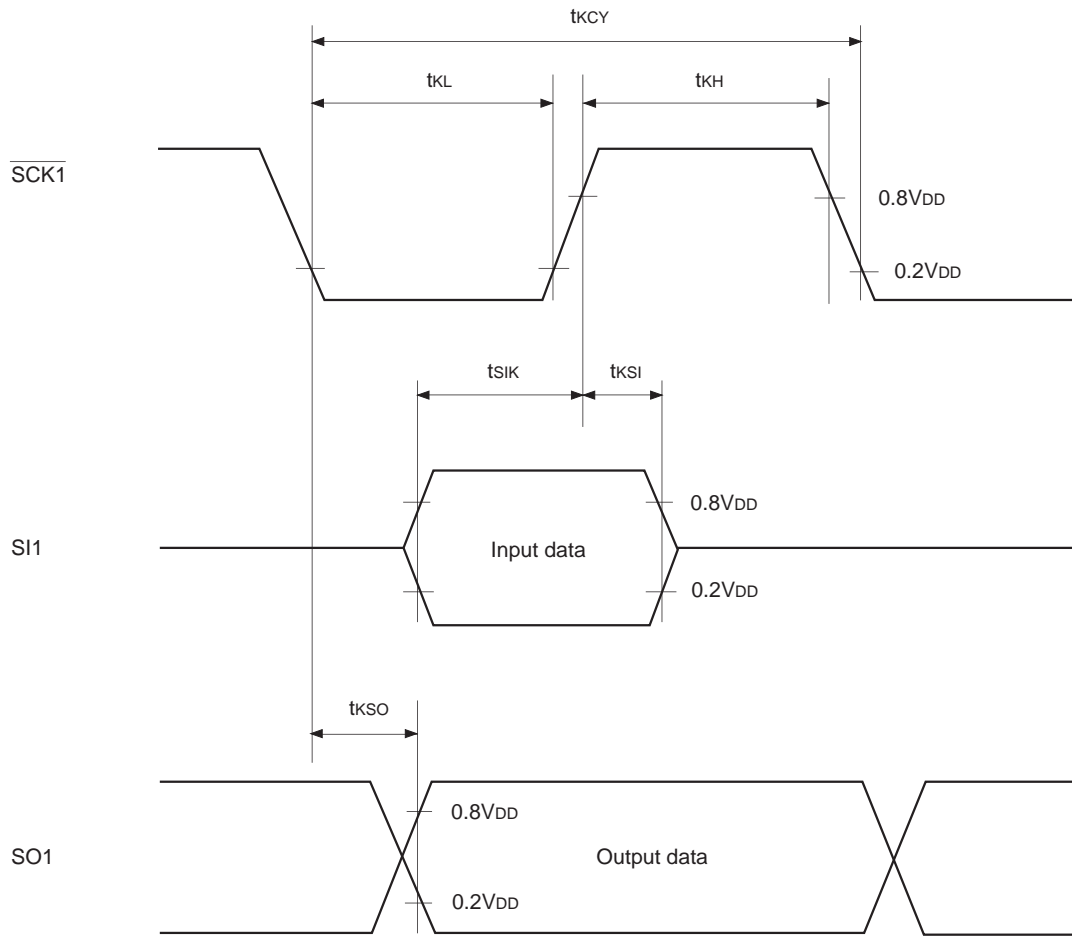
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}}+200$		ns
			Output mode	$16000/f_c$		ns
SCK1 high and low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}}+100$		ns
			Output mode	$8000/f_c-150$		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	$t_{\text{SIK}}$	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	$t_{\text{KSI}}$	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}}+200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	$t_{\text{KSO}}$	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}}+250$	ns
			$\overline{\text{SCK1}}$ output mode		125	ns

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{\text{sys}}$  [ns]=2000/ $f_c$  (Upper 2 bits="00"), 4000/ $f_c$  (Upper 2 bits="01"), 16000/ $f_c$  (Upper 2 bits="11")

**Note 2)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing (SIO mode)



**Serial transfer (CH1) (Special mode)**

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	$t_{LCY}$	SO1 SI1	Note 1)		104		$\mu\text{s}$
SI1 data setup time	$t_{LSU}$	SI1		2			$\mu\text{s}$
SI1 data hold time	$t_{LHD}$	SI1		2			$\mu\text{s}$

**Note 1)**  $t_{LCY}$  specifies only serial mode register (CH1) (SIOM1: Address 01FAH) lower 2 bits (SO1 clock selection) has been set at  $104\mu\text{s}$ .

**Note 2)** The load of SO1 pin is  $50\text{pF} + 1\text{TTL}$ .

**Serial transfer (CH1) (Special mode)**

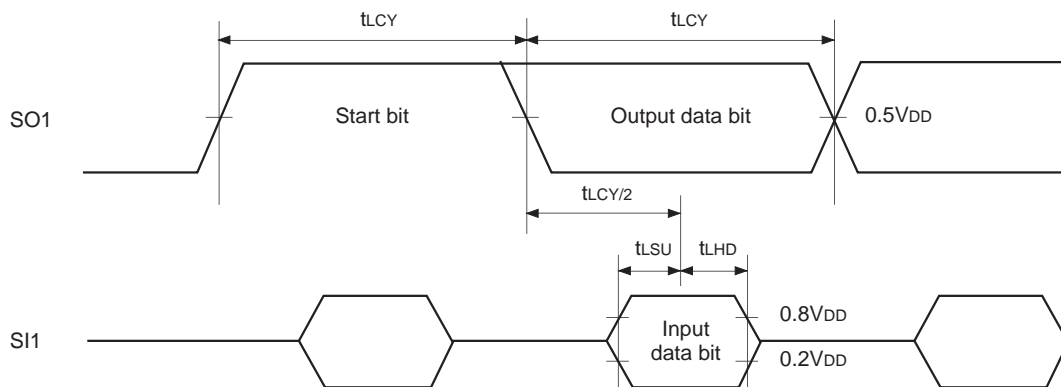
( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 3.0$  to  $3.6\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	$t_{LCY}$	SO1 SI1	Note 1)		104		$\mu\text{s}$
SI1 data setup time	$t_{LSU}$	SI1		2			$\mu\text{s}$
SI1 data hold time	$t_{LHD}$	SI1		2			$\mu\text{s}$

**Note 1)**  $t_{LCY}$  specifies only serial mode register (CH1) (SIOM1: Address 01FAH) lower 2 bits (SO1 clock selection) has been set at  $104\mu\text{s}$ .

**Note 2)** The load of SO1 pin is  $50\text{pF}$ .

**Fig. 6. Serial transfer CH1 timing (Special mode)**



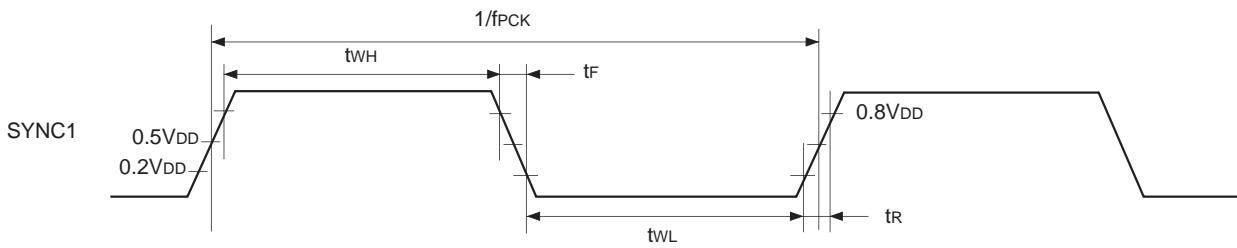


**(3) General purpose prescaler**

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	$f_{PCK}$	SYNC1				12	MHz
External clock input pulse width	$t_{WH}$ , $t_{WL}$	SYNC1		33			ns
External clock input rise and fall times	$t_R$ , $t_F$	SYNC1				200	ns

**Fig. 7. General purpose prescaler timing**



(4) HSYNC counter

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 3.0$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

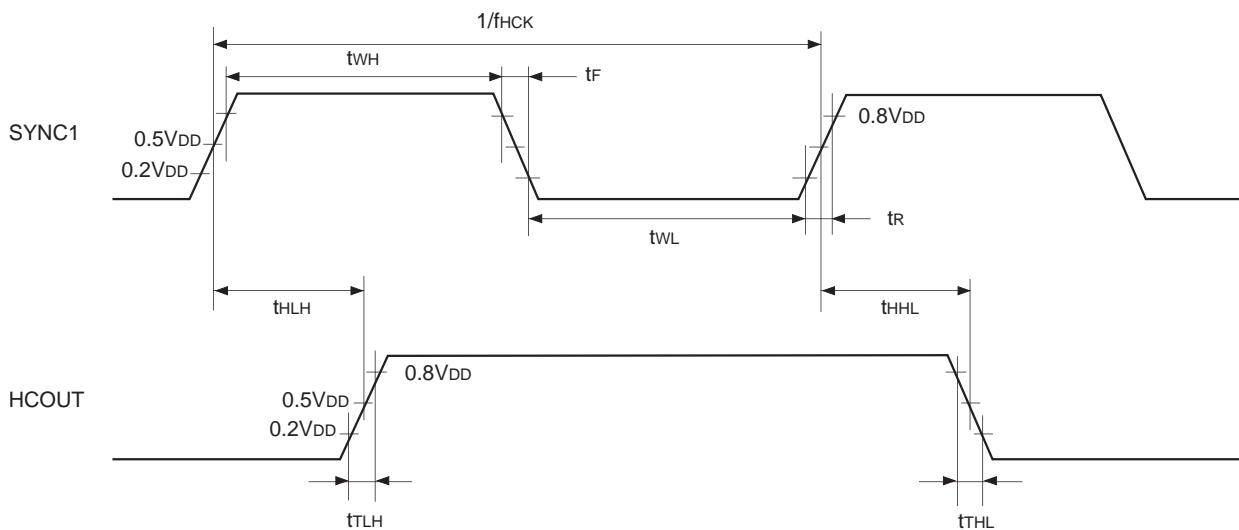
Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	$f_{HCK}$	SYNC1				12	MHz
External clock input pulse width	$t_{WH}$ , $t_{WL}$	SYNC1		33			ns
External clock input rise and fall times	$t_R$ , $t_F$	SYNC1				200	ns
HCOUT output delay time (against SYNC1 $\uparrow$ )	$t_{HLH}$ , $t_{HHL}$	HCOUT	External clock input SYNC1 $t_R = t_F = 6\text{ns}$		$t_{sys} + 130$	$t_{sys} + 220$	ns
HCOUT output rise and fall times	$t_{TLH}$	HCOUT	External clock input SYNC1 $t_R = t_F = 6\text{ns}$		24	50	ns
	$t_{THL}$				12	25	ns

**Note1)**  $t_{sys}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$$t_{sys} [\text{ns}] = 2000/f_c \text{ (Upper 2 bits = "00")}, 4000/f_c \text{ (Upper 2 bits = "01")}, 16000/f_c \text{ (Upper 2 bits = "11").}$$

**Note2)** The load of HCOUT pin is 50pF.

Fig. 8. HSYNC counter timing



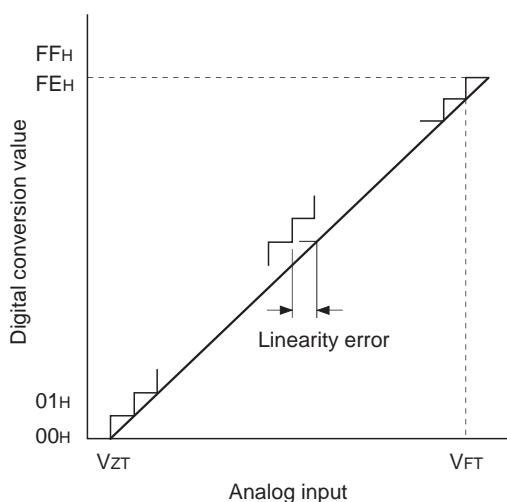
(5) A/D converter characteristics (Ta=-10 to +75°C, VDD=AVDD=4.5 to 5.5V, AVREF=4.0 to AVDD, VSS=AVSS=0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta=25°C VDD=AVDD=AVREF=5.0V VSS=AVSS=0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t <sub>CONV</sub>			160/f <sub>ADC</sub> *			µs
Sampling time	t <sub>SAMP</sub>			12/f <sub>ADC</sub> *			µs
Reference input voltage	V <sub>REF</sub>	AV <sub>REF</sub>	VDD=AVDD=4.5 to 5.5V	AVDD-0.5		AVDD	V
Analog input voltage	V <sub>IAN</sub>	AN0 to AN11		0			V
AV <sub>REF</sub> current	I <sub>REF</sub>	AV <sub>REF</sub>	Operating mode		0.6	1.0	mA
	I <sub>REFS</sub>		SLEEP mode STOP mode 32kHz operating mode			10	µA

(Ta=-10 to +75°C, VDD=AVDD=3.0 to 3.6V, AVREF=2.7 to AVDD, VSS=AVSS=0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta=25°C VDD=AVDD=AVREF=5.0V VSS=AVSS=0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t <sub>CONV</sub>			160/f <sub>ADC</sub> *			µs
Sampling time	t <sub>SAMP</sub>			12/f <sub>ADC</sub> *			µs
Reference input voltage	V <sub>REF</sub>	AV <sub>REF</sub>	VDD=AVDD=3.0 to 3.6V	AVDD-0.3		AVDD	V
Analog input voltage	V <sub>IAN</sub>	AN0 to AN11		0			V
AV <sub>REF</sub> current	I <sub>REF</sub>	AV <sub>REF</sub>	Operating mode		0.4	0.7	mA
	I <sub>REFS</sub>		SLEEP mode STOP mode 32kHz operating mode			10	µA

Fig. 9. Definitions of A/D converter terms



\* The value of f<sub>ADC</sub> is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).

When PS2 is selected, f<sub>ADC</sub>=fc/2

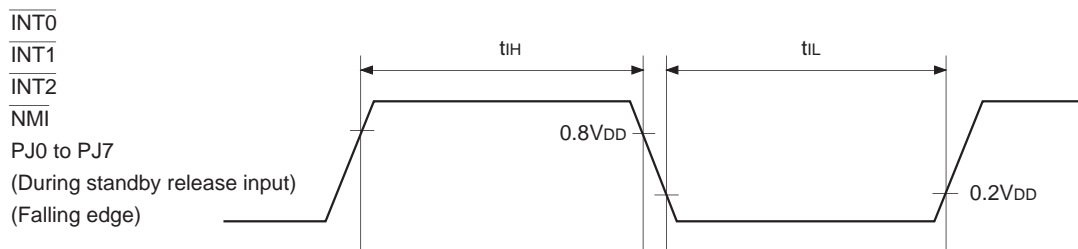
When PS1 is selected, f<sub>ADC</sub>=fc

**(6) Interruption, reset input**

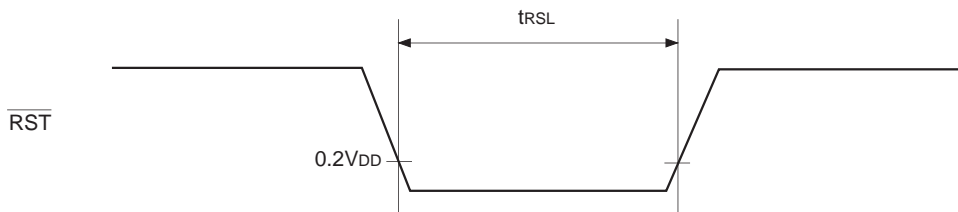
( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 3.0$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	$t_{IH}$ $t_{IL}$	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ NMI PJ0 to PJ7		1		$\mu\text{s}$
Reset input low level width	$t_{RSL}$	$\overline{\text{RST}}$		$32/f_c$		$\mu\text{s}$

**Fig. 10. Interruption input timing**



**Fig. 11. Reset input timing**



**(7) Others**

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 3.0$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

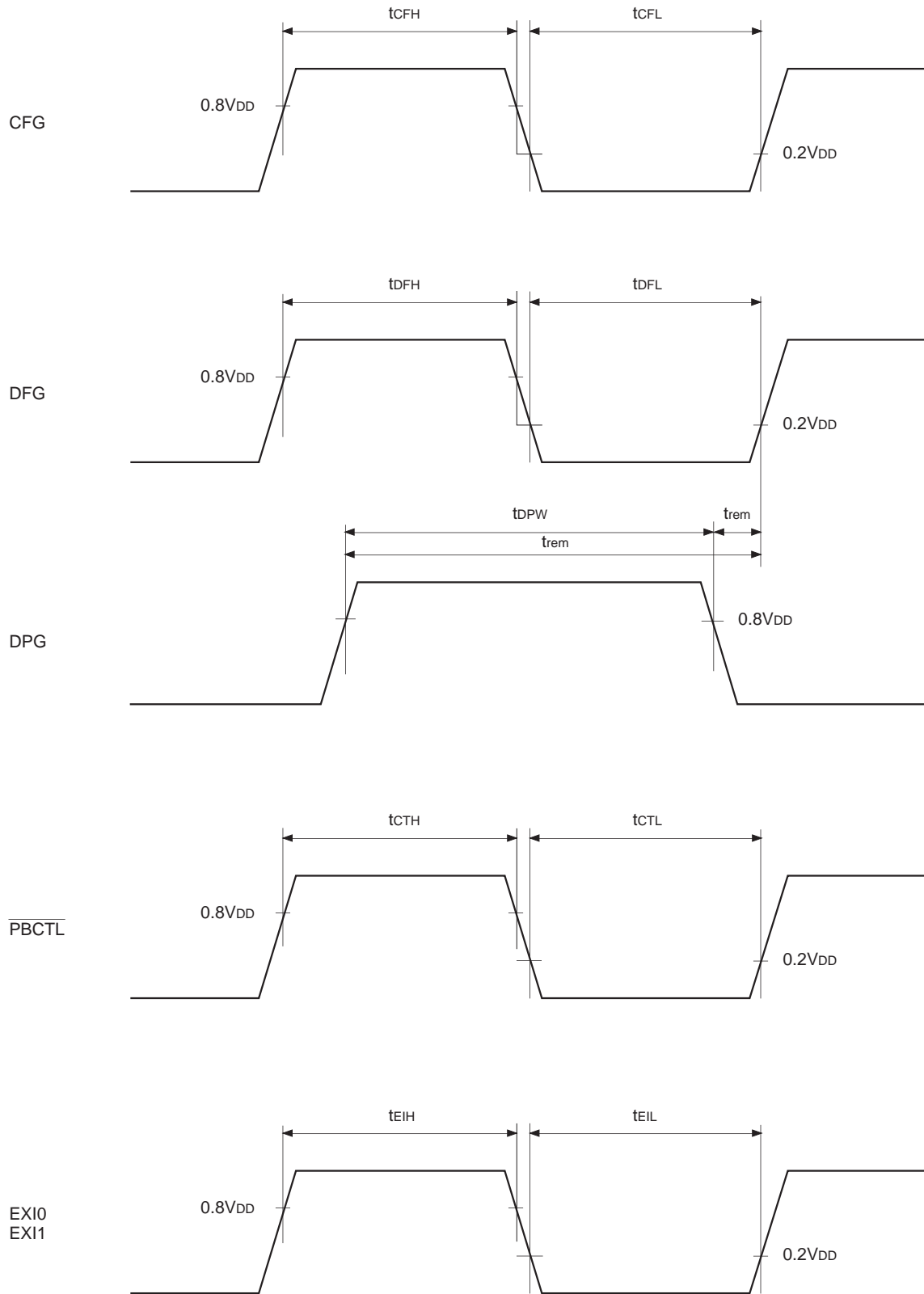
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input high and low level widths	$t_{CFH}$ $t_{CFL}$	CFG		$t_{FRC} \times 24 + 200$		ns
DFG input high and low level widths	$t_{DFH}$ $t_{DFL}$	DFG		$t_{FRC} \times 16 + 200$		ns
DPG minimum pulse width	$t_{DPW}$	DPG		$t_{FRC} \times 8 + 200$		ns
DPG minimum removal time	$t_{rem}$	DPG		$t_{FRC} \times 16 + 200$		ns
$\overline{\text{PBCTL}}$ input high and low level widths	$t_{CTH}$ $t_{CTL}$	$\overline{\text{PBCTL}}$	$t_{sys} = 2000/f_c$	$t_{FRC} \times 8 + 200 + t_{sys}$		ns
EXI input high and low level widths	$t_{EIH}$ $t_{EIL}$	EXI0 EXI1	$t_{sys} = 2000/f_c$	$t_{FRC} \times 8 + 200 + t_{sys}$		ns

**Note)**  $t_{sys}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{sys}$  [ns] =  $2000/f_c$  (Upper 2 bits = "00"),  $4000/f_c$  (Upper 2 bits = "01"),  $16000/f_c$  (Upper 2 bits = "11")

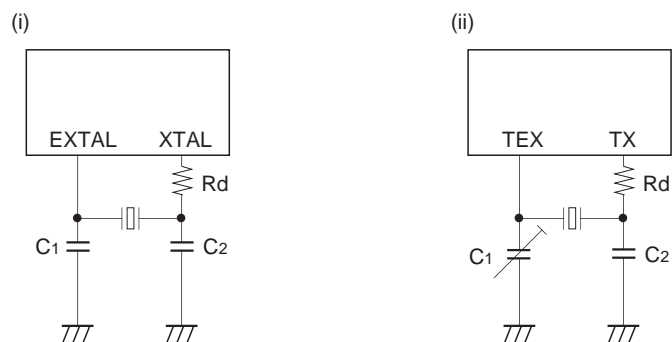
$t_{FRC} = 1000/f_c$  [ns]

Fig. 12. Other timings



Supplement

Fig. 13. Recommended oscillation circuit



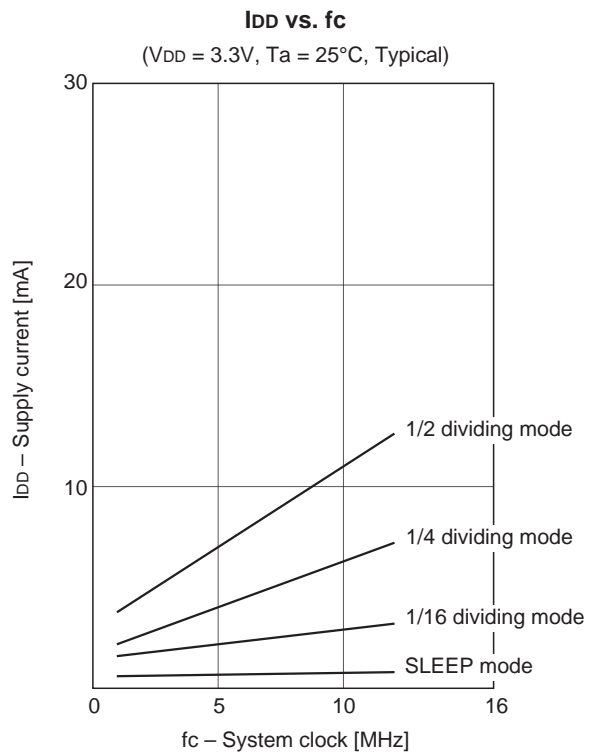
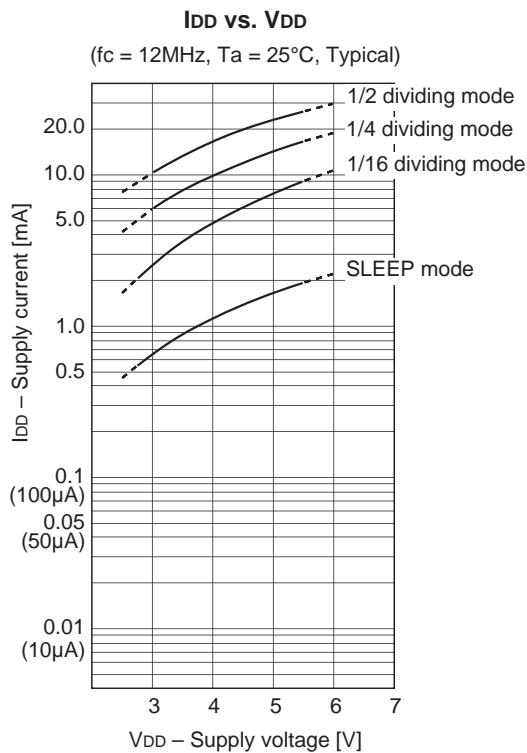
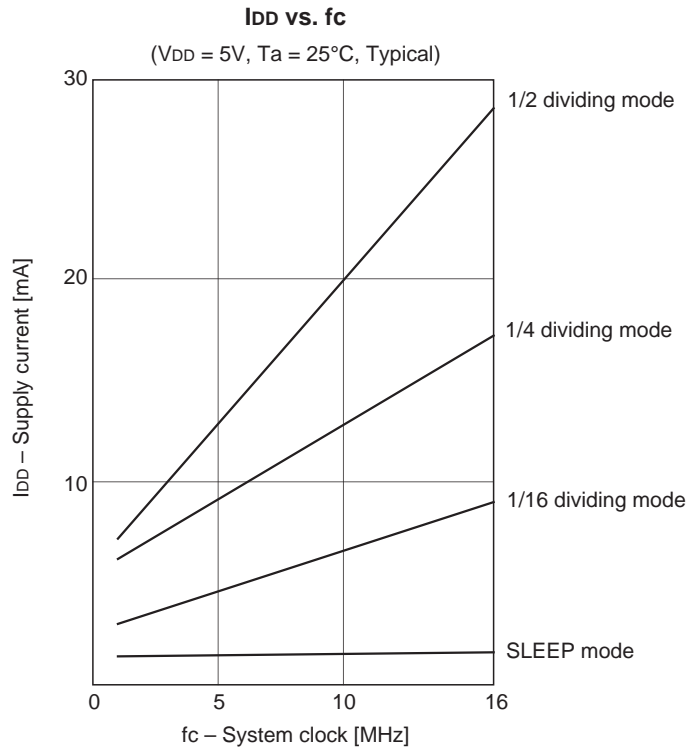
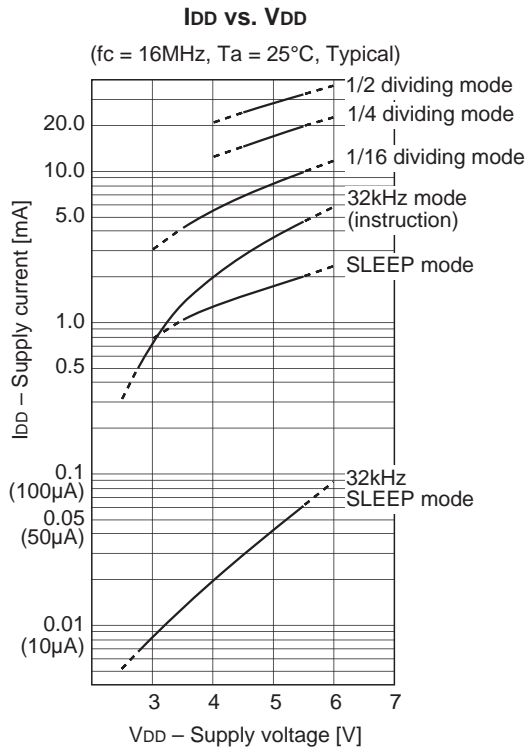
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

Selection Guide

Option item	Mask product	CXP873P60Q-1 -□□□	CXP873P60R-1 -□□□	CXP873P60Q-2 -□□□	CXP873P60R-2 -□□□
Package	100-pin plastic QFP/LQFP	100-pin plastic QFP	100-pin plastic LQFP	100-pin plastic QFP	100-pin plastic LQFP
ROM capacitance	52K byte /60K byte	PROM 60K byte	PROM 60K byte	PROM 60K byte	PROM 60K byte
Reset pin pull-up resistor	Existent /Non-Existent	Existent	Existent	Existent	Existent
Input circuit format*	CMOS schmitt /TTL schmitt	TTL schmitt	TTL schmitt	CMOS schmitt	CMOS schmitt

\* Pins PG4/SYNC0, PG5/SYNC1 only.

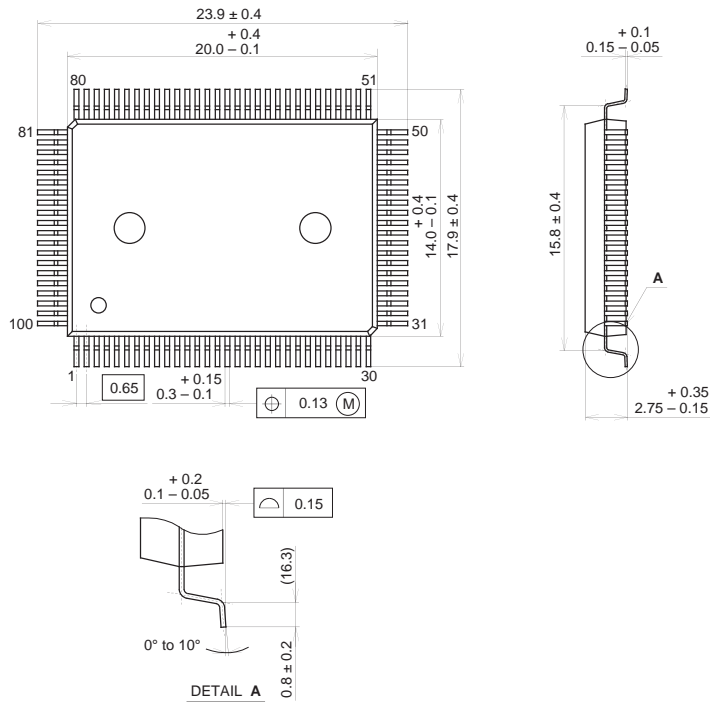
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

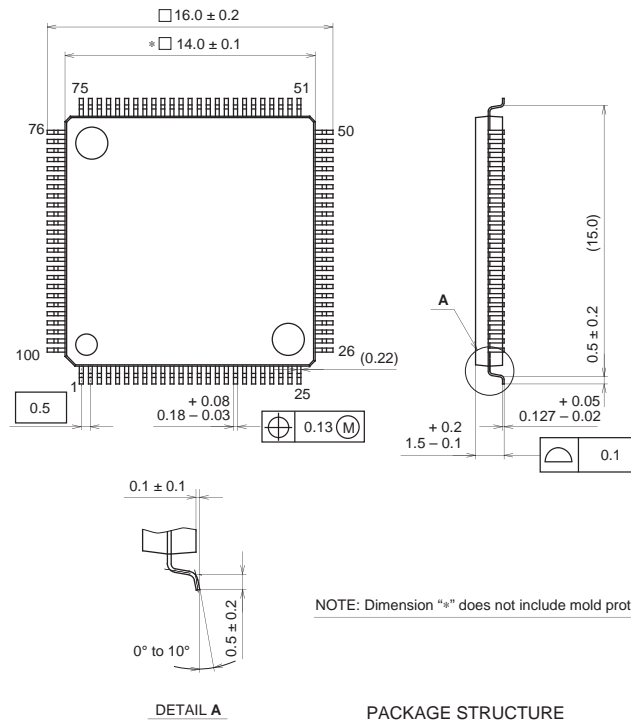


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN LQFP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	LQFP100-P-1414
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g